REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Office Action dated 16 October 2007.

In the Office Action, Claims 1-17 were indicated as allowed. The allowance of Claims 1-17 is acknowledged and appreciated.

Claims 20, 24, 25, 27 and 31-33 were objected to in the Office Action, however, the Examiner indicated that these Claims would be allowable if rewritten in independent form including all the limitations of the base Claim and any intervening Claims.

Further, in the Official Action, Claims 18-19, 21-23, 26, and 28-30 were rejected under 35 U.S.C. §103(a) as being unpatentable over Chen, et al. (U.S. Patent Publication No. 2002/0158862); in view of Koyama, et al. (U.S. Patent No. 5,680,149).

Chen, et al. is directed to a central symmetric gamma voltage correction circuit which is formed by two resistors, a varistor and two buffers. An external voltage V_{cc} is divided by resistors R_a and R_b, and a varistor V_R as shown in Fig. 4 of Chen, et al. When resistance values of the resistors R_a and R_b are equal, by adjusting the resistance of the varistor V_R, symmetrical output voltages ($V_{th}+$) and ($V_{th}-$) are acquired from two ends of the varistor V_R.

In the present device, a current source provides a reference current, which in conjunction with an adjustable resistor and reference voltage, supplies a plurality of gamma currents I_S, via a current mirror 30. These features are completely missing in Chen, et al.

Further, in contrast to the claimed arrangement, in Chen, et al., the central symmetric gamma voltage correction circuit generates a positive polarity correction voltage (V_{th}+) and a negative polarity correction voltage (V_{th}-) at two ends in the varistor V_R.

In the present device, a common gamma voltage V_{GCOM} is generated by the unit 102 and the amplifier 114, as shown in Figure 3 of the present Patent Application. The generated V_{GCOM} is output to the mirror mapping circuit to serve at the axis of symmetry for the plurality of gamma voltages V_{G1}-V_{G5} supplied to the mirror mapping circuit 136, and the gamma voltages V_{G6}-V_{G10} which are output from the mirror mapping circuit. This feature is never presented in Chen, et al.

The Examiner has noted that Chen, et al. fails to disclose a current source and a current mirror; and cited the Koyama, et al. Patent as employing a current source and a current mirror. It is respectfully submitted that although Koyama, et al. refers to the mirror circuit constructed by N-channel TFTs 106 and 107, this reference, however, fails to teach or suggest the mirroring of the reference current supplied by the current source to generate a plurality of gamma currents, as is the case in the present device.

The present device specifically generates a plurality of gamma currents I_s which are employed to individually produce variable first gamma voltages. The buffer circuit of Koyama, et al. does not provide such a plurality of gamma currents. Moreover, it would not be obvious to combine Koyama's buffer circuit with the Chen device since the Chen buffers output voltages at 201, whereas the present invention uses gamma currents to provide first gamma voltages.

What is more, the Chen device requires multiple external reference voltages to be input at buffers 201 in the driver circuit 20 (paragraph [0028], bottom). In contradistinction, the present invention requires only one reference voltage V_{ref} to be supplied at current source 46, to further aid in generating all of the first gamma voltages.

Lastly, the present invention provides for independent and automatic tuning of the second gamma voltages. When the first gamma voltages V_{G1}-V_{G5} are tuned by varying any of R_{com} or R_1-R_5, the mirror mapping circuit 136 acts to automatically tune the second gamma voltages V_{G6}-V_{G10} (paragraph [0016]). Thus, symmetry of the first and second gamma voltages is assured regardless of changes in the first gamma voltages. Such automatic tuning is not taught by Chen or Koyama.

Therefore, neither the Chen et al., nor Koyama et al. reference teaches or discloses "...a gamma voltage generator for generating a plurality of individually and automatically tuned gamma voltages..." and "...said means for generating said common gamma voltage and a plurality of first and second gamma voltages including a mirror mapping circuit coupled to said common gamma voltage and first gamma voltages, to generate the plurality of said second gamma voltages; whereby tuning the plurality of first gamma voltages automatically tunes the plurality of second gamma voltages...", as is now recited in newly amended independent Claim 18. Nor do Chen or Koyama teach or disclose "A method for generating a plurality of individually and automatically tuned gamma voltages..." and "...establishing a mirror mapping circuit coupled to said common gamma voltage and first gamma voltages, for automatically tuning the plurality

of second gamma voltages in response to a tuning of the plurality of first gamma voltages...", as is now recited in newly amended independent Claim 26.

Therefore, since the references fail to suggest the combination of elements that form the invention of the subject Patent Application, they are not believed to make obvious that invention.

Claims 19-25, dependent on Claim 18, and Claims 27-33, dependent on Claim 26, are believed to be allowable for at least the reason of their dependency on what is believed to be an allowable Claim.

It is now believed that the subject Patent Application has been placed in condition for allowance, and such action is respectfully requested.

If there are any further charges associated with this filing, the Honorable Commissioner for Patents is hereby authorized to charge Deposit Account #18-2011 for such charges.

Respectfully submitted,
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